

23

be formed on the third insulating layer **243** to cover the first and second barrier patterns **258** and **268** and the first interconnection **278**. The second interconnection layer may include the same material as or different material from the first interconnection **278**. Fourth semiconductor photolithography and etching processes may be performed on the second interconnection layer.

A photoresist pattern may be formed on the second interconnection using the fourth semiconductor photolithography process. The photoresist pattern may overlap the third interconnection structure **298** of the second active region **64** of FIG. 7. By using the photoresist pattern and the third insulating layer **243** as an etch mask and an etch buffer layer, respectively, the fourth semiconductor etching process may be performed on the second interconnection layer. The second interconnection layer may be etched using the fourth semiconductor etching process to expose the third insulating layer **243**, thereby forming the second interconnection **288**.

The second interconnection **288** may constitute the third interconnection structure **298** along with the first and second barrier patterns **258** and **268** and the first interconnection **278**. The third interconnection structure **298** may be included in a CMOS transistor **300** according to embodiments of the inventive concept. The connection hole **245** may be formed on each of the first, third, and fourth active regions **62**, **66**, and **68**, the first interconnection structure **153**, **156**, or **159**, and the second interconnection structure **223**, **226**, or **229** as shown in FIG. 7.

The third interconnection structure **298** may be formed in the connection hole **245** formed in each of the first, third, and fourth active regions **62**, **66** and **68**, the first interconnection structure **153**, **156**, or **159**, and the second interconnection structure **223**, **226**, or **229**. In this case, the third interconnection structure **298** may be in contact with a top surface of the first interconnection structure **153**, **156**, or **159**. The third interconnection structure **298** may be in contact with a top surface of the second interconnection structure **223**, **226**, or **229**.

Embodiment 9

FIG. 20 is a schematic cross-sectional view taken along line III-III' of FIG. 7, illustrating a method of forming a CMOS transistor, according to embodiments of the inventive concept. In FIG. 20, the same reference numerals are used to denote the same elements as in FIG. 19.

Referring to FIG. 20, according to embodiments of the inventive concept, a connection hole **245** may be formed in the semiconductor substrate **50** and the third insulating layer **243** of FIG. 19. The connection hole **245** may extend under a top surface of a second active region **64** through the third insulating layer **243**. The connection hole **245** may be formed on each of first, third, and fourth active regions **62**, **66**, and **68**, first interconnection structure **153**, **156**, or **159**, and second interconnection structure **223**, **226**, or **229** as shown in FIG. 7.

The third interconnection structure **298** of FIG. 19 may be formed on the third insulating layer **243** to fill the connection hole **245**. The third interconnection structure **298** of the second active region **64** may be included in a CMOS transistor **300** according to embodiments of the inventive concept. The third interconnection structure **298** may be formed in each of the first, third, and fourth active regions **62**, **66**, and **68**, the first interconnection structure **153**, **156**, or **159**, and the second interconnection structure **223**, **226**, or **229**.

In this case, the third interconnection structure **298** may be partially inserted into the first interconnection structure **153**, **156**, or **159** through a top surface of the first intercon-

24

nection structure **153**, **156**, or **159**. The third interconnection structure **298** may be partially inserted into the second interconnection structure **223**, **226**, or **229** through a top surface of the second interconnection structure **223**, **226**, or **229**.

FIG. 21 is a schematic plan view of a semiconductor module including a semiconductor device of FIG. 7.

Referring to FIG. 21, a semiconductor module **330** according to embodiments of the inventive concept may include a module substrate **320**. The module substrate **320** may be a printed circuit board (PCB), or a plate including an electrical circuit. The module substrate **320** may include internal circuits (not shown), electrical pads (not shown), and connectors **329**. The internal circuits may be electrically connected to the electrical pads and the connectors **329**. Semiconductor package structures **315** and at least one resistor **323** may be disposed on the module substrate **320**.

Alternatively, the semiconductor package structures **315**, the at least one resistor **323**, and at least one condenser **326** may be disposed on the module substrate **320**. The semiconductor package structures **315** may be electrically connected to the electrical pads along with the at least one resistor **323** and/or the at least one condenser **326**. Each of the semiconductor package structures **315** may include at least one semiconductor device **310**, which may include at least one CMOS transistor **300** of FIG. 7.

The CMOS transistor **300** may include a p-type impurity diffusion region **54** and an n-type impurity diffusion region **58**. The p-type impurity diffusion region **54** may include the first and second active regions **62** and **64** of FIG. 7 in the semiconductor substrate **50** of FIG. 9. The first active region **62** may include the first interconnection structure **153**, **156**, or **159** of FIG. 7. The selected third interconnection structures **294** or **298** of FIG. 7 may be disposed on the first and second active regions **62** and **64** and the first interconnection structure **153**, **156**, or **159**.

The n-type impurity diffusion region **58** may include the third and fourth active regions **66** and **68** of FIG. 7 in the semiconductor substrate **50** of FIG. 9. The third active region **66** may include the second interconnection structure **223**, **226**, or **229** of FIG. 7. The remaining third interconnection structures **294** or **298** may be disposed on the third and fourth active regions **66** and **68** and the second interconnection structure **223**, **226**, or **229**. Thus, the semiconductor module **330** may have better electrical properties than in the conventional art.

The semiconductor module **330** may be electrically connected to the processor-based system **370** of FIG. 22 through the connectors **329** of the module substrate **320**.

FIG. 22 is a schematic plan view of a processor-based system including a semiconductor device of FIG. 7.

Referring to FIG. 22, a processor-based system **370** according to embodiments of the inventive concept may include at least one system board (not shown). The at least one system board may include at least one bus line **365**. A first module unit may be disposed on the at least one bus line **365**. The first module unit may be electrically connected to the at least one bus line **365**.

The first module unit may include a central processing unit (CPU) **343**, a floppy disk drive (FDD) **346**, and a compact disk read-only-memory (ROM) drive **349**. Also, a second module unit may be disposed on the at least one bus line **365**. The second module unit may be electrically connected to the at least one bus line **365**.

The second module unit may include a first input/output (I/O) device **352**, a second I/O device **354**, a ROM **356**, and a random access memory (RAM) **358**. The RAM **358** may